

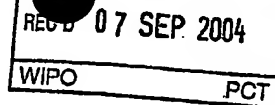
PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT



(PCT Article 36 and Rule 70)

10/519346



Applicant's or agent's file reference DASP/76000.WO/B	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/PEA416)	
International application No. PCT/IB 03/02380	International filing date (day/month/year) 19.06.2003	Priority date (day/month/year) 21.06.2002
International Patent Classification (IPC) or both national classification and IPC G01R31/3185		
Applicant MELEXIS NV et al.		

<p>1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 38.</p> <p>2. This REPORT consists of a total of 5 sheets, including this cover sheet.</p> <p><input checked="" type="checkbox"/> This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of <u>5</u> sheets.</p>																									
<p style="text-align: right;">EPO - DG 1</p> <p>3. This report contains indications relating to the following items: 01.11.2004</p> <table border="0"> <tr> <td>I</td> <td><input checked="" type="checkbox"/></td> <td>Basis of the opinion</td> </tr> <tr> <td>II</td> <td><input type="checkbox"/></td> <td>Priority</td> </tr> <tr> <td>III</td> <td><input type="checkbox"/></td> <td>Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</td> </tr> <tr> <td>IV</td> <td><input type="checkbox"/></td> <td>Lack of unity of invention</td> </tr> <tr> <td>V</td> <td><input checked="" type="checkbox"/></td> <td>Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</td> </tr> <tr> <td>VI</td> <td><input type="checkbox"/></td> <td>Certain documents cited</td> </tr> <tr> <td>VII</td> <td><input type="checkbox"/></td> <td>Certain defects in the international application</td> </tr> <tr> <td>VIII</td> <td><input type="checkbox"/></td> <td>Certain observations on the international application</td> </tr> </table>		I	<input checked="" type="checkbox"/>	Basis of the opinion	II	<input type="checkbox"/>	Priority	III	<input type="checkbox"/>	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability	IV	<input type="checkbox"/>	Lack of unity of invention	V	<input checked="" type="checkbox"/>	Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement	VI	<input type="checkbox"/>	Certain documents cited	VII	<input type="checkbox"/>	Certain defects in the international application	VIII	<input type="checkbox"/>	Certain observations on the international application
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Date of submission of the demand 20.01.2004	Date of completion of this report 01.09.2004
Name and mailing address of the international preliminary examining authority:  European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Hijazi, A Telephone No. +49 89 2399-7782 

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT**

International application No. **PCT/IB 03/02380**

I. Basis of the report

1. With regard to the elements of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17):*

Description, Pages

1-8 as originally filed

Claims, Numbers

5, 6 filed with telefax on 30.03.2004
1-4 filed with telefax on 22.06.2004

Drawings, Sheets

1/9-9/9 filed with telefax on 22.06.2004

2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
☐ the language of publication of the international application (under Rule 48.3(b)).
☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
☐ filed together with the international application in computer readable form.
☐ furnished subsequently to this Authority in written form.
☐ furnished subsequently to this Authority in computer readable form.
☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
☐ the claims, Nos.:
☐ the drawings, sheets:

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EXAMINATION REPORT**

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5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	1-6
	No: Claims	
Inventive step (IS)	Yes: Claims	1-6
	No: Claims	
Industrial applicability (IA)	Yes: Claims	1-6
	No: Claims	

2. Citations and explanations

see separate sheet

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International application No. PCT/IB 03/02380

1. Reference is made to the following documents:

D1: PATENT ABSTRACTS OF JAPAN vol. 006, no. 230 (E-142), 16 November 1982 &

D1a: JP 57 133656 A (NIPPON DENKI KK), 18 August 1982

2 Article 34(2)(b) PCT.

2.1 New claim 1 is supported by the originally filed claim 1 in combination with claim 5.

2.2 New claim 3 is supported by line 18 on page 2 of the description.

2.3 New claims 5 and 6 are supported by lines 16-20 on page 4 of the description

3 Article 6 PCT.

The expression "absence of positive action" used in claim 1 is vague and unclear and leaves the reader into doubt as to the meaning of the technical feature to which it refers, thereby rendering the definition of the subject-matter of said claim unclear (Article 6 PCT). Indeed, neither a "positive action" is defined in the claim nor after how much time it is decided that there is an "absence", and therefore the meaning of the claim is not clear from the wording of the claim alone for the person skilled in the art (Guidelines 5.31). For the purpose of drafting this report, the expression "absence of positive action" will be understood as being that the voltage at the single input/output pin is held below a logical level "low" for a period of time determined by an "escape 0 timer" (see description page 4, lines 18-20).

4 Article 33(2) and (3) PCT.

Independent claim 1

4.1 D1 is considered to be the closest prior art and discloses an arrangement aiming to reduce the number of pins necessary for testing an IC.

4.2 The subject-matter of claim 1 (interpreted in the light of paragraph 3) mainly differs from D1 in that the change from test mode to normal mode is decided by monitoring if the voltage at the single input/output pin is held below a logical level "low" for a period of time determined by an "escape 0 timer". The subject-matter of

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claim 1 is therefore new in the sense of Article 33(2) PCT.

- 4.3 D1 is only mentioning that a test mode condition is maintained until a reset signal R is inputted. No precision is given in D1 as to how this signal is generated, the word "input" could even be said as conveying the idea that the reset signal is applied through another input terminal. The timeout aspect leading to the switching from test mode to normal mode is not mentioned in any of the cited document of the Internal Search Report. No Incentive could be found in D1 as to why the skilled person would use a timeout in order to reset the circuit after testing and therefore the subject-matter of claim 1 is considered to involve an inventive step in the sense of Article 33(3) PCT.

Dependent claims

- 4.4 **Claims 2-6** depend on claim 1 and are therefore also new and inventive in the sense of Article 33(2) and (3) PCT.

5 Article 33(4) PCT.

All the claims are related to an integrated circuit and therefore are considered to be industrially applicable.

25. 01. 2005

CLAIMS

(41)

1. An integrated circuit comprises one or more integrated circuit elements and one or more input/output pins, the one or more integrated circuit elements including an interface element for interfacing with external test circuitry, the interface element communicating with the external test circuitry via a single input/output pin dedicated for testing wherein the single pin connected operates with several logic thresholds and wherein the absence of positive action from the external test circuitry the integrated circuit defaults from test mode to normal mode.
2. An integrated circuit according to Claim 1 wherein the interface element is embedded into the integrated circuit as a single pin interface between the digital integrated circuit and the external test circuitry.
3. An integrated circuit according to Claim 2 wherein the interface element receives test data and commands from the external test circuitry in response to which a scan path block controls and commands scan path elements within the digital integrated circuit and returns the resulting data to the external test circuitry.
4. An integrated circuit according to any preceding Claim wherein the logic thresholds define several logic levels which enable data and timing signals to be differentiated on a single pin.